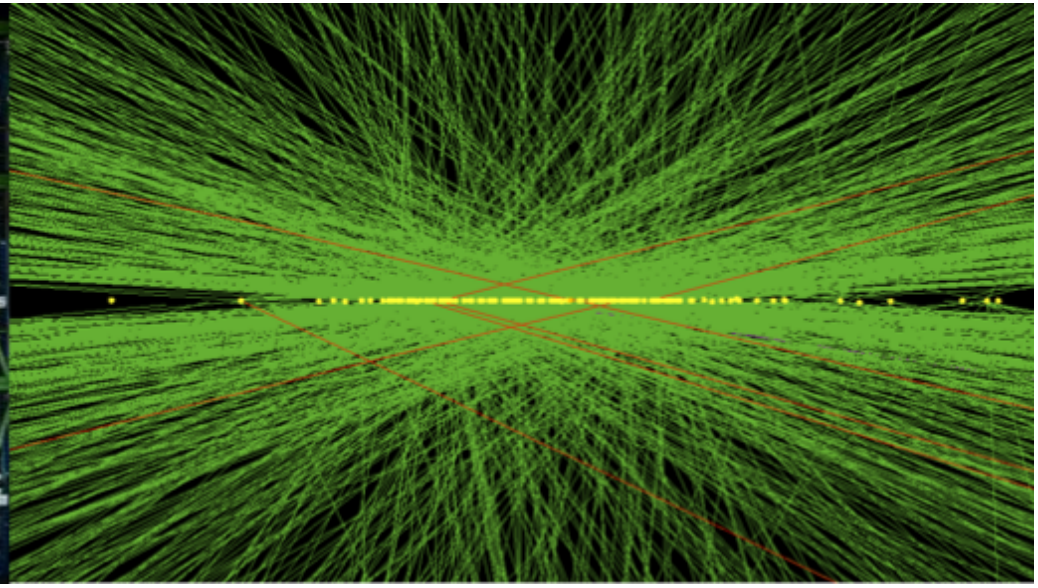
B03: BTL Concentrator Card

Yurii Maravin
Kansas State University

HL-LHC CMS CD-1 Review

23 October 2019



Biographical sketch

- Yurii Maravin, professor at Kansas State University
- Roles in USCMS MTD:
  - L4 US-CMS manager of the BTL Electronics Concentrator Card section: design, production and testing, as well as the delivery of the BTL Concentrator Cards
- Experience:
  - CMS since 2005
  - HCAL Calibration co-convener
  - ECAL Calibration co-convener, EGM POG co-convener
  - Physics: SMP, EXO, Higgs
  - Cosmic Ray Veto Front end board production and testing for mu2e experiment

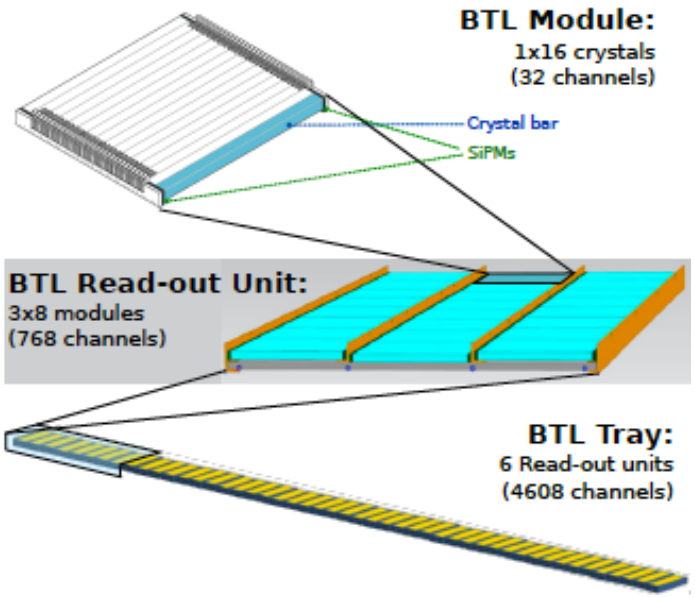
Outline

- Scope and Deliverables of 402.8.3.3
- Conceptual Design
- QA/QC
- Cost
- Milestones
- Risks
- Summary
- Backup
  - Environmental, Safety and Health
  - Value Engineering/Resource Optimization
  - Responses to Previous Reviews

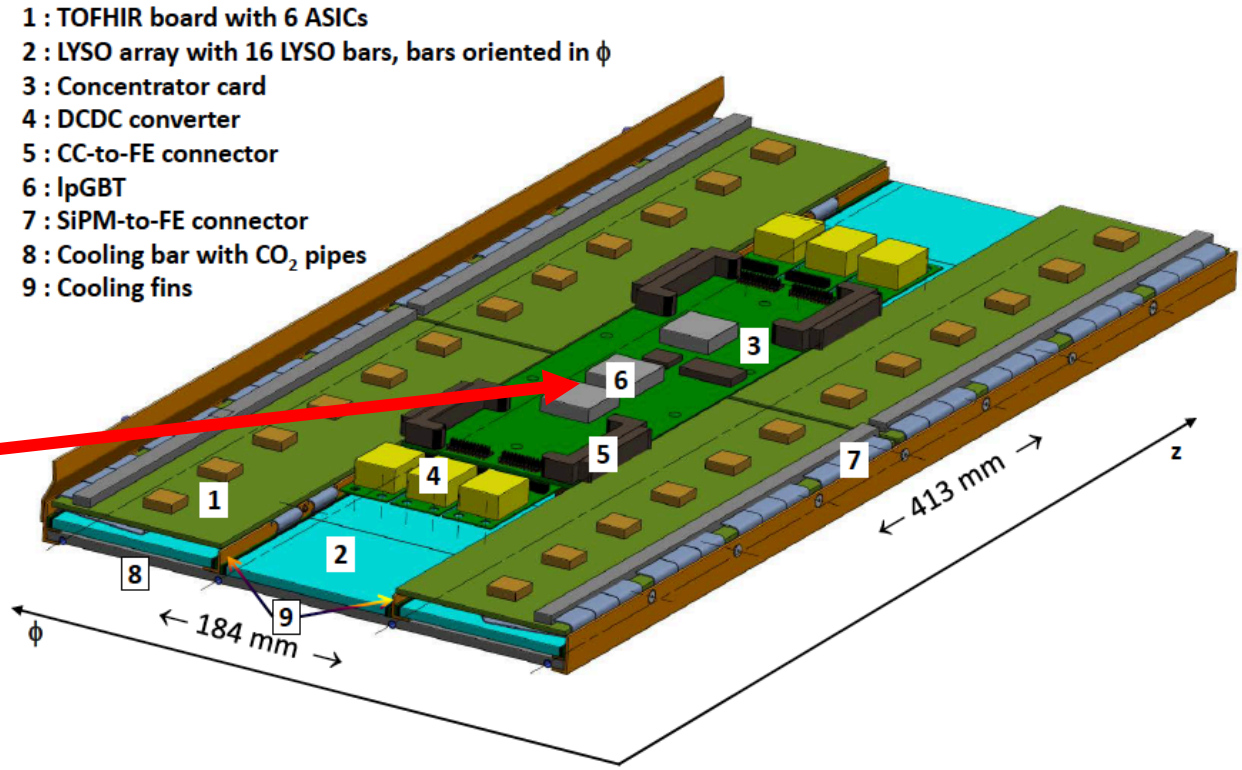
Scope and Deliverables for 402.8.3.3

- Concentrator Card 402.8.3.3 :
  - Design the concentrator card
  - Procure necessary materials and assemble the boards
    - Split in three stages: prototype, pre-production, and production
  - Design both testing protocol and test bench to ensure functionality and quantify the effect of aging on the board performance (temperature, magnetic, and radiation)
- Deliver 100% of the Concentrator Card for the BTL project (432 boards + 10% spares)

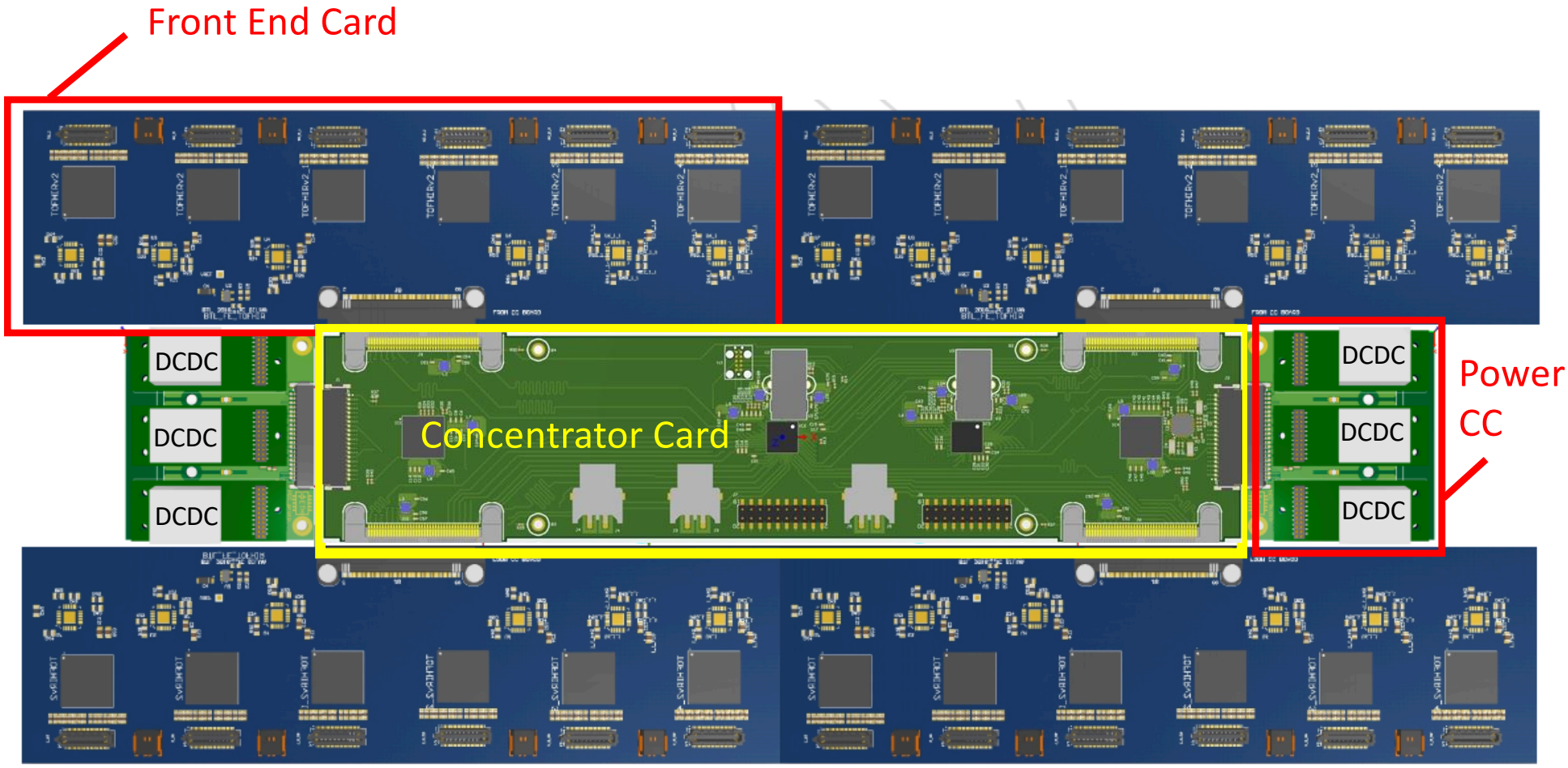
BTL and Readout Unit



- BTL: 72 trays: 2 in z and 36 in ϕ
- Readout Unit: Front End electronics that process data from 1/6th of a tray
  - Total of 432 Readout Units are needed
- Readout Unit:
  - 4 Front End cards host TOFHIR ASICs to process SiPM signals
  - **Concentrator card** provides power, data i/o, control, slow monitoring



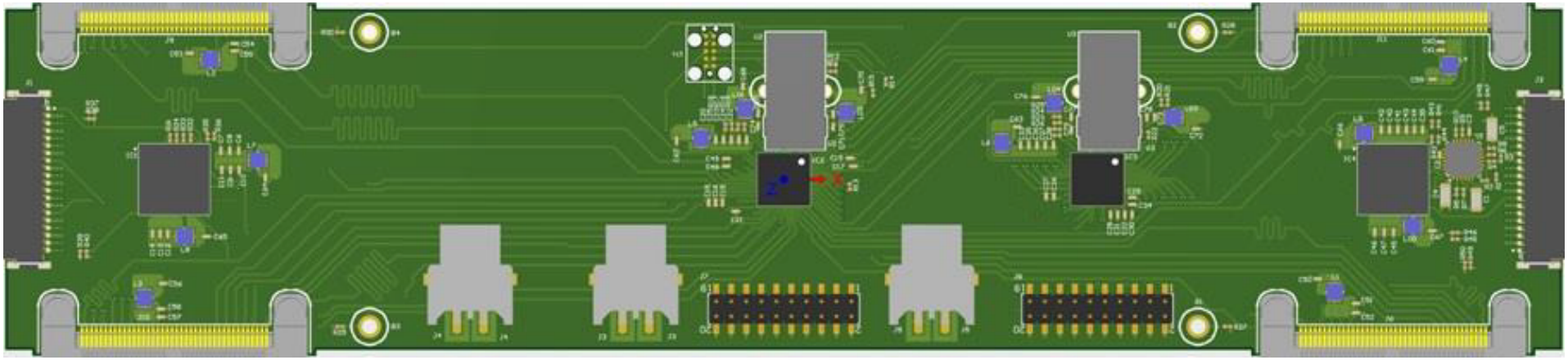
Readout Unit



- Three main components:
  - Four front end cards: signal processing
  - Two power concentrator card: power supply to the readout unit
  - Concentrator card: routing power, data i/o, slow control monitoring

Concentrator Card functions

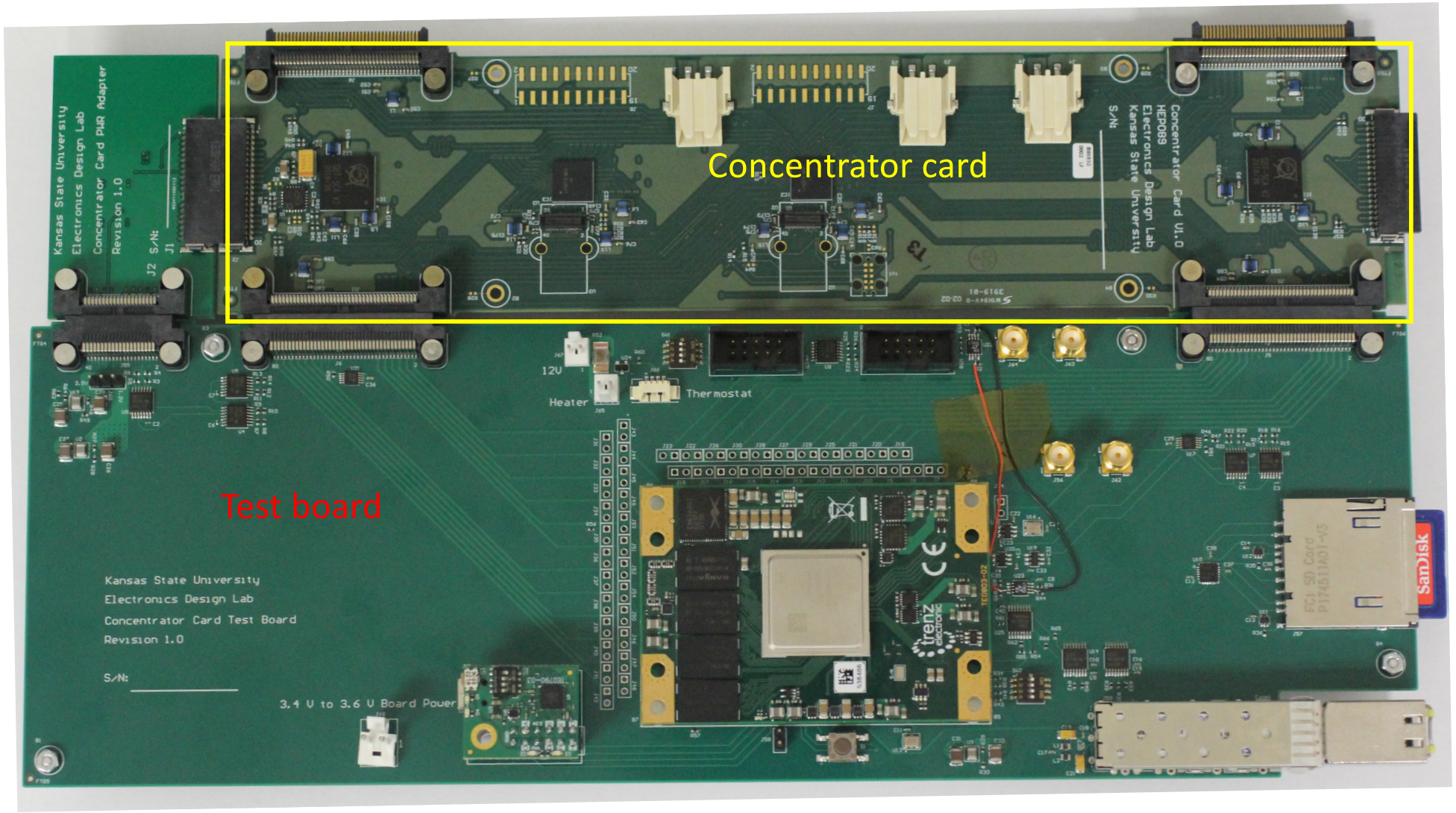
- Concentrator card is an integral part of the BTL electronics readout unit
  - Data concentration to a 10.24 Gb/s fiber to the back-end
  - Dedicated fiber to provide timing information to TOFHIR2
  - 2.56 Gb/s downlink from back-end
  - Supply voltage, temperature, bias voltage monitoring using lpGBT and two GBT-SCA ASICs
  - ALDO2 control through lpGBT and GBT-SCA GPIO



Timeline for the CC development

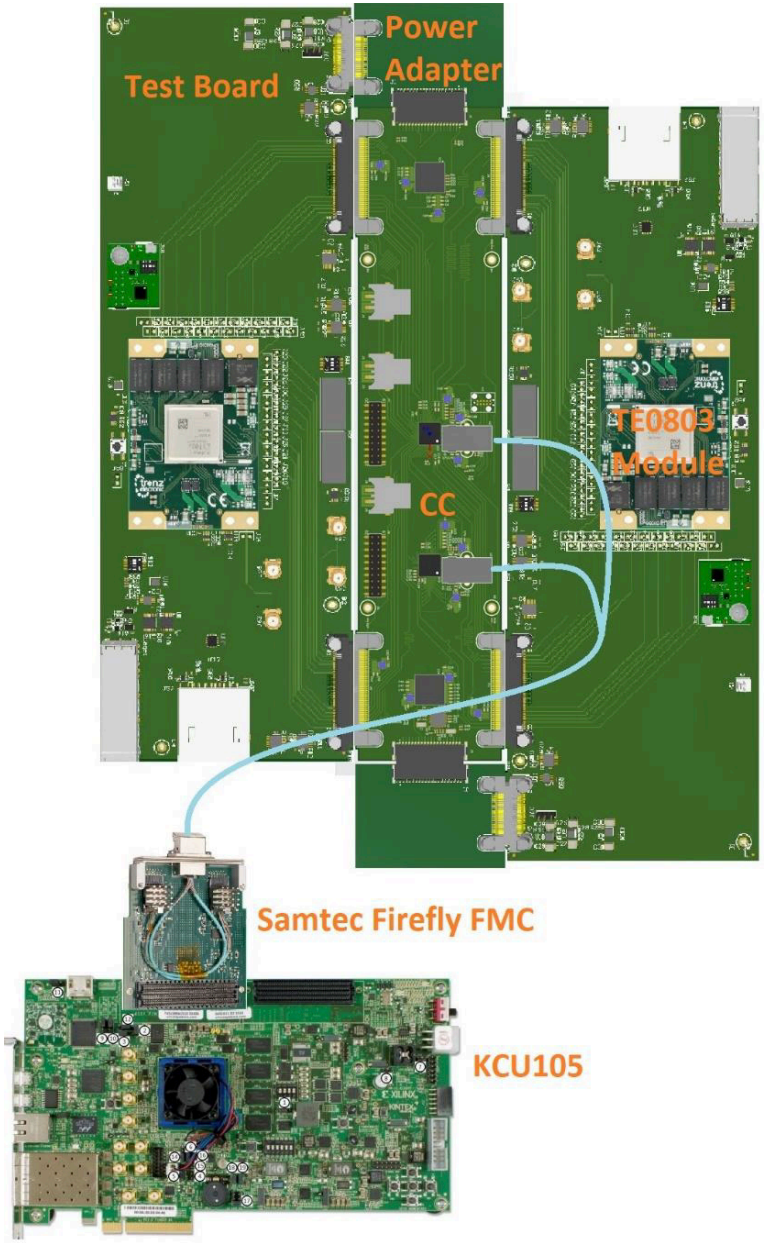
- Power only prototype: CY Q1 – Q3 2018
  - No I/O option, study power distribution/thermal dissipation
- RUproto1: CY Q4 2018 – Q4 2019
  - CC board with core functionality as in final system
    - Allows for mechanical integration with final detector module prototypes
    - Interface to DAQ close to final system
- RUproto2: CY Q3 2019 – Q1 2021
  - Finalizing the design for production
- Production: CY Q2 2021 – Q2 2022
  - TOFHIRv2 ASIC readiness: Q1 2021
  - Clock distribution finalized: Q2 2021

RUproto1 CC is at KSU!



Testing concentrator cards

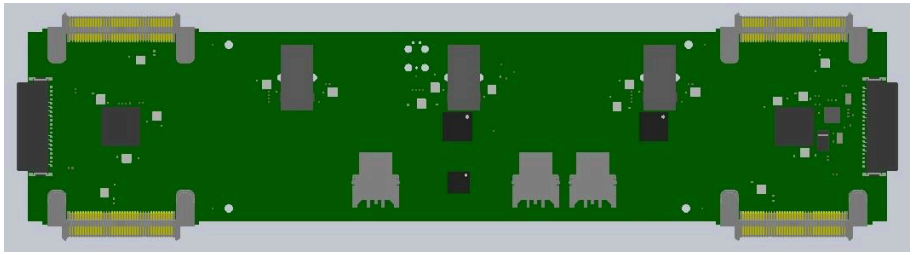
- Independent verification of the CC assembly and functionality
  - KCU105 FPGA board for back-end communication
  - Trenz TE0803 Zynq Ultrascale+ for FE IO simulation
- Scalable for additional testing throughput
- Aging testing planned
  - Temp cycling
  - Burn in
  - Magnetic field
  - Radiation hardness



Charges #1, 3, 5

Design Updates

- RUproto1 is 2 lpGBT/2 VTRX+ design
- RUproto2 implementation is close to complete pending some final choices
  - Options:
    - Possible additional VTRX+ for dedicated clock distribution
    - Possible additional lpGBT to allow to use its internal PLL to clean up clock jitter
    - Possible consolidation of PCC onto CC's PCB
    - Designs accommodating each of these options are already complete
  - Decisions will be made well ahead of June 2020 component order

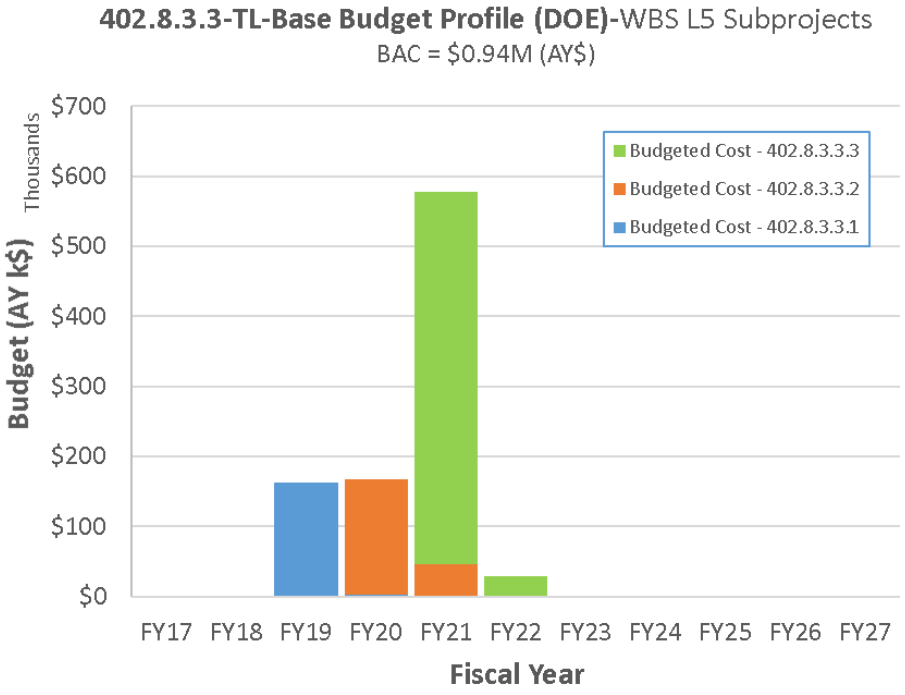


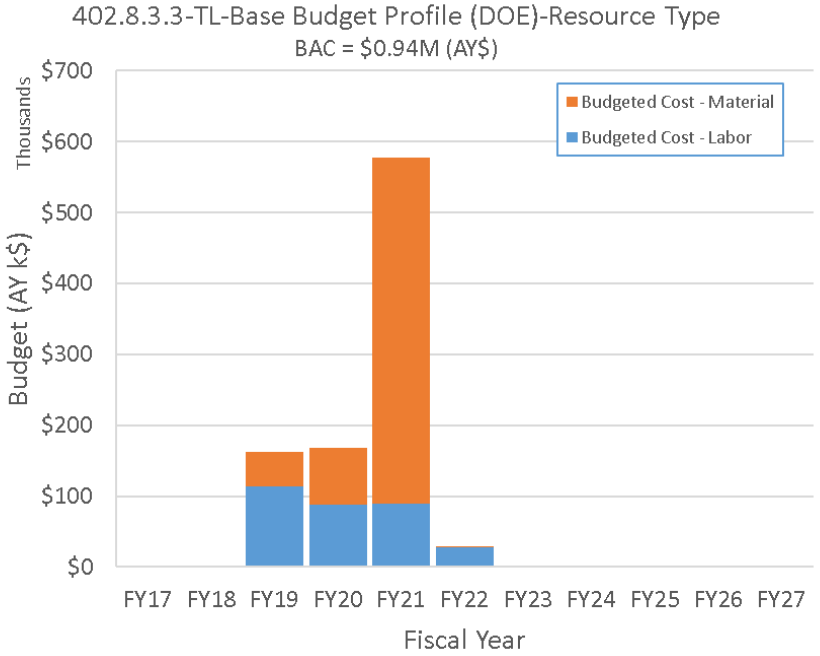
- Production concentrator card design
  - Final design depends on final choices that will be made that impact the multiplicity of lpGBT/VTRX+ chips
    - Decision on provision of L0 trigger to MTD
    - Redundancy in clock distribution
    - Insurance on clock quality
  - These choices affect the component cost for the production-era CC. For now we include in our planning a risk threat encapsulating these possibilities and their impact on the production-era CC (see more in a few slides)

Costs

CMS-doc-13509
CMS-doc-13591

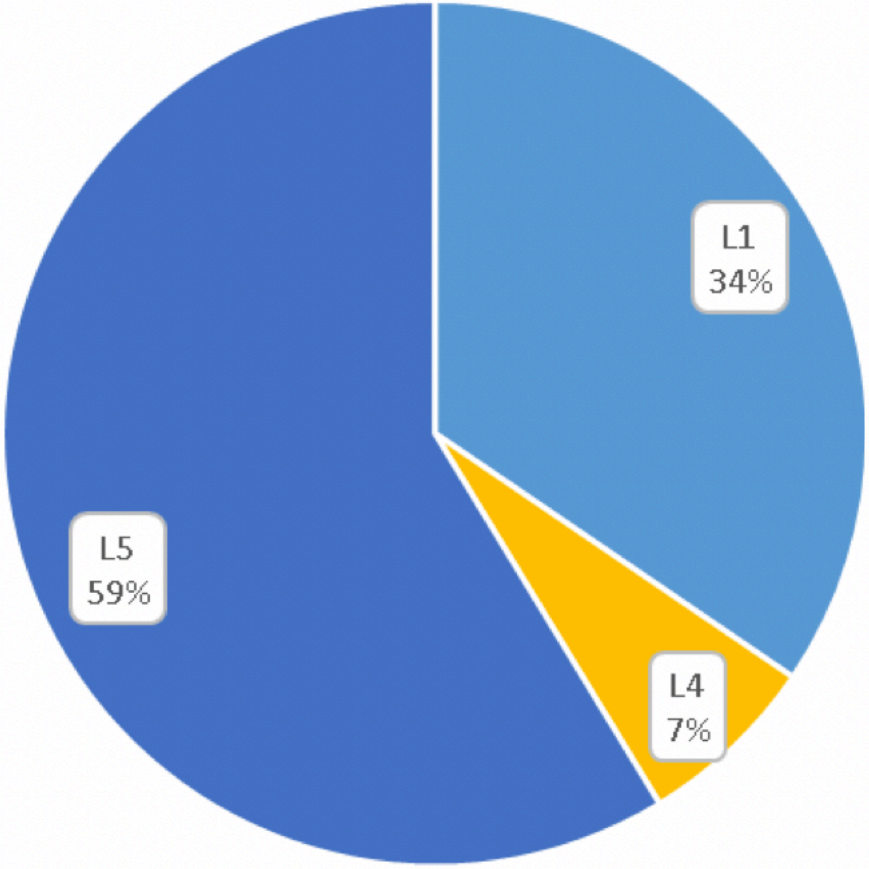
- Detailed description, including vendor quotes can be found in BoE (CMS-doc-13591)
- Profile cost for L5 areas as well as the that for M&S and labor are given below (left and right, respectively)

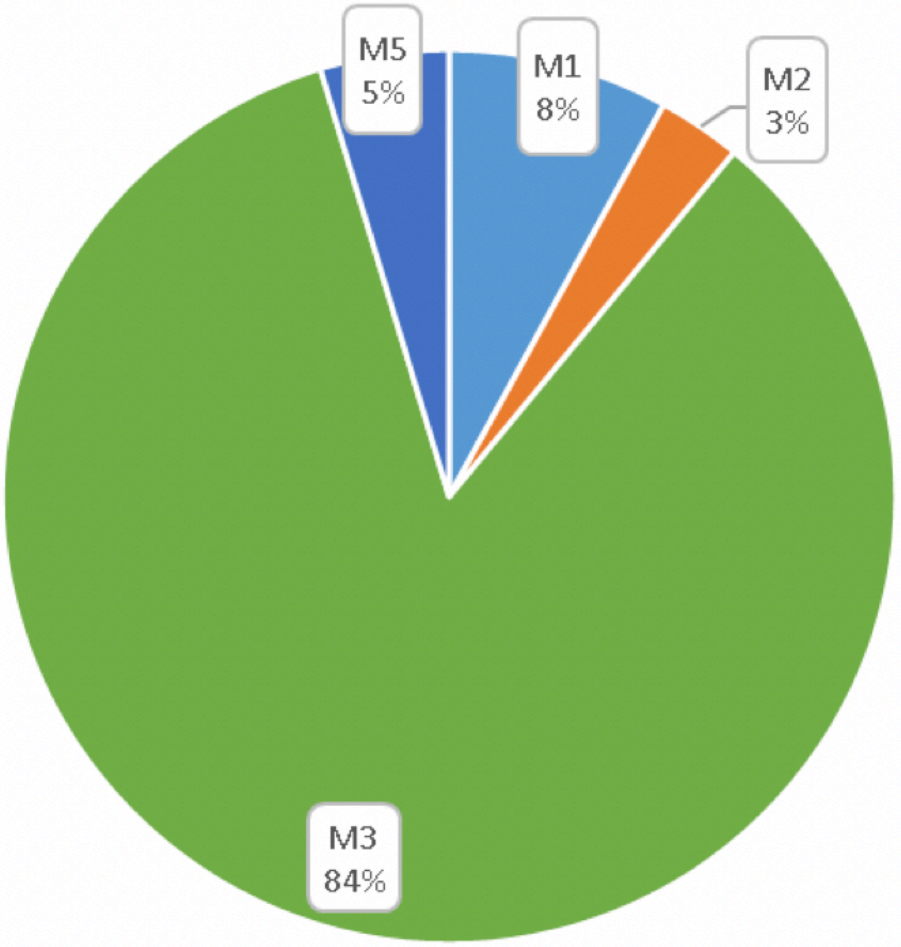




Costs (continued)

- Estimate uncertainty breakdowns for labor and M&S (left and right, respectively)





Risks

CMS-doc-13480

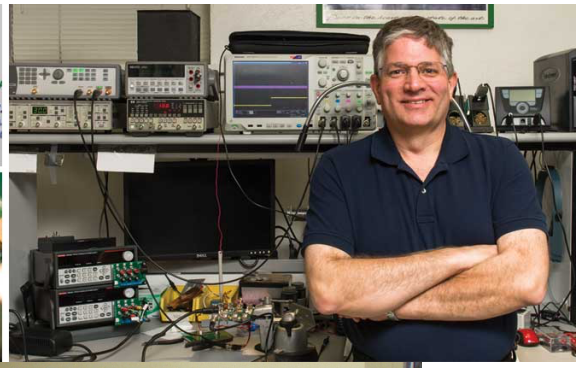
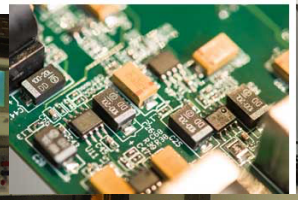
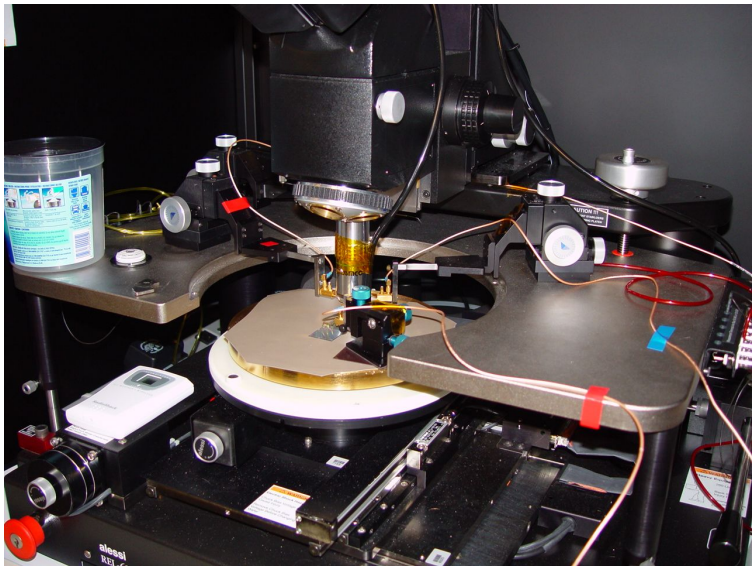
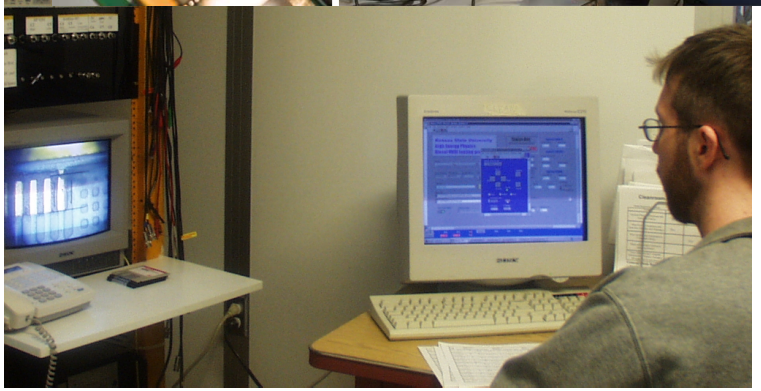
WBS / Ops Lab Activity : 402.8 TL - Timing Layer (general risks) (2)				
Risk Rank : 2 (Medium) (1)				
RT-402-8-91-D	TL - Shortfall in Timing Layer scientific labor	30 % 0 -- 0 -- 611 k$	0 months	61
Risk Rank : 1 (Low) (1)				
RT-402-8-90-D	TL - Key Timing Layer personnel need to be replaced	25 % 45 -- 135 -- 261 k$	0 -- 0 -- 3 months	37
WBS / Ops Lab Activity : 402.8.3 BTL - Barrel Timing Layer (14)				
Risk Rank : 3 (High) (2)				
RT-402-8-30-D	BTL - Concentrator Card requires significant design changes	50 % 40 -- 135 -- 175 k$	1 -- 3 -- 6 months	58
RT-402-8-07-D	BTL - Concentrator Card delay in external component deliveries	50 % 50 k$	3 -- 6 -- 9 months	25
Risk Rank : 2 (Medium) (4)				
RT-402-8-05-D	BTL - Change in interfaces of tray assembly components	20 % 150 -- 250 -- 350 k$	3 months	50
RT-402-8-46-D	BTL - Problems with sensor gluing facility	50 % 90 k$	1 -- 2 -- 3 months	45
RT-402-8-33-D	BTL - Difficulties procuring LYSO from international suppliers	10 % 100 -- 250 -- 400 k$	3 -- 6 -- 9 months	25
RT-402-8-14-D	BTL - Problems with SiPM vendor	20 % 32 -- 96 -- 128 k$	2 -- 6 -- 8 months	17
Risk Rank : 1 (Low) (8)				
RT-402-8-15-D	BTL - Batch shipment of SiPMs lost in transport	5 % 224 k$	1 months	11
RT-402-8-35-D	BTL - Delays or damage of tray in transport to CERN	5 % 220 k$	1 months	11
RT-402-8-04-D	BTL - LYSO matrices not meeting specifications	10 % 100 k$	1 -- 2 -- 3 months	10
RT-402-8-36-D	BTL - Interface to iCMS changes	20 % 30 k$	1 -- 2 -- 3 months	6
RT-402-8-34-D	BTL - Delay in delivery of components from iCMS	20 % 10 -- 20 -- 30 k$	1 -- 2 -- 3 months	4
RT-402-8-18-D	BTL - Concentrator card production & testing facility problem	20 % 10 k$	0.5 -- 1 -- 2 months	2
RT-402-8-08-D	BTL - Delay in cooling plate delivery	10 % 10 -- 20 -- 30 k$	1 -- 2 -- 3 months	2
RT-402-8-42-D	BTL - Problems with module assembly site	10 % 10 -- 20 -- 30 k$	1 -- 2 -- 3 months	2

Decisions will be made well ahead of June 2020 component order

- RT-402-8-30-D: BTL – Concentrator card requires significant design changes
  - Covers possible component count changes for production cards discussed previously
  - Additional yet-unforeseen design changes could impact the completion of the CC R&D and prototyping
  - Close coordination with international BTL electronics effort to ensure coherence
- RT-402-8-07-D: BTL – Concentrator card delay in external component deliveries
  - CC is not on the critical path, but a large delay in components could affect downstream activities
  - Example: lpGBT delivery schedule recently redefined (Sept 2019 update) as 6 month later than implementation in P6 – we can accommodate this delay but a longer delay puts the CC on the critical path for BTL assembly

QA and QC Testing

- KSU Electronic Design Laboratory: several decades of work for HEP experiments
  - D0 SMT, CMS Pixel phase 1 and 2 upgrade work, CMS HCAL phase 1 upgrade work, mu2e CRV FEB production and testing, Double Chooz, protoDUNE, DUNE 35t
- The QC facility in the US at Kansas State University
  - Testing facility: 50 m^2 class 10000 (ISO 7) clean room
  - Batch testing of the CCs by undergraduate students

Collaborating institutions

- CMS (US-CMS)
  - Kansas-State University (KSU Electronic design laboratory)
    - Russell Taylor: two decade long experience in designing, producing, testing HEP hardware (D0 silicon detector, CMS Pixel phase 1 and 2 upgrade, CMS HCAL phase 1 upgrade, mu2e CRV FEB production and testing)
    - David Huddlestone: experience with vendors, procuring components
  - Interface very close to non-US collaborations
    - LIP: Front End Boards, TOFHIRv2
    - Milano: power regulator ALDO2
    - ETH: Power concentrator cards (PCC)
    - CERN: lpGBT, VTRX+, GBT-SCA

Summary

- The first power-only prototype has already been built and used in TOFHiR tests in LIP
- Prototype RUproto1 boards arrived at KSU early this month and testing has already began
  - First prototype of the test bench is ready
- CC design is prepared and prototypes are already being tested
- Potential changes are small and designs are ready for each option

Backup

Environmental, Safety and Health

- In General Safety is achieved through standard Lab/Institute practices
  - No construction, accelerator operation, or exotic fabrication
  - No imminent peril situations or unusual hazards
  - Items comply with local safety standards in site of fabrication and operation
  - Site Safety officers at Institutes identified in the SOW
- There are no Specific Hazards for 402.8.3.3
  - No high voltage/radiation risks are present in QC/QA program at K-State laboratory
  - Risks associated with this project are typical to those found in labs pursuing electronic design
- All ES&H aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Safety Management approach, and the rules and procedures laid out in the Fermilab ES&H Manual
- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394)

Opportunities for Value Engineering

- Experience with multiple vendors
- Significant testing infrastructure at K-State
  - Thermal units, test station, numerous equipment to allow manual tests if needed
- Access to well-trained electrical engineering students working at K-State Electronic Design Laboratory to assist with testing

Responses to Previous Reviews p1

From Director's review, May 2019

Status: closed

- BTL-R3: Consider setting granularity of number of chips/card so that one DC-DC converter is matched to a single TOFHIR readout card
  - The current design takes this suggestion into account by assigning a single DC-DC converter per single TOFHIR readout card. Thus, four DC-DC converters serve four TOFHIR card, and the remaining two are used to power the Concentrator Card
- BTL-R4: Develop a plan for powering up the ASICs card connected to the concentrator card and for exploiting the lpGBT capabilities for control and environmental monitoring

Responses to Previous Reviews p2

From Director's review, May 2019

Status: closed

- BTL-R4: Develop a plan for powering up the ASICs card connected to the concentrator card and for exploiting the lpGBT capabilities for control and environmental monitoring
  - The capabilities for powering up/down, control, and environmental monitoring are given below. They allow full control to implement powering up/powering down scheme that will be designed together with the detector control specialists and MTD teams. Each FE board DC-DC converter enable will be controlled from a GBT-SCA GPIO pin. The PGood signal from each DC-DC converter will be monitored by a GBT-SCA GPIO pin. Each DC-DC converter output voltage will be monitored by a GBT-SCA analog input. The board input voltage will be monitored by a GBT-SCA analog input. The temperature of the PCC and FE boards will be monitored by a GBT-SCA analog input. Four SiPM temperature sensors will be monitored by the LpGBT analog inputs. Total bias current for every 16 SiPM's will be monitored by GBT-SCA analog inputs (12 from each FE board). Internal temperature sensors in each GBT-SCA (2) and each LpGBT (2) will monitor temperature of the CC.